深圳市深科电子有限公司

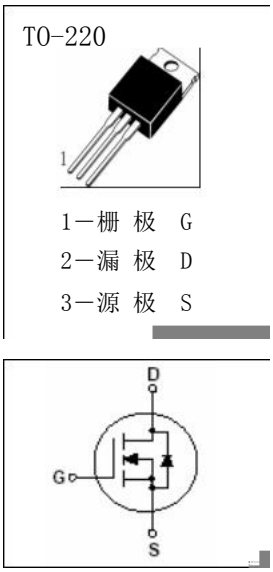
N-Channel Enhancement Mode Field Effect Transistor

# STS100N03L

## ■ 主要用途

高速开关应用。DC/DC转换器、电源管理等。

## ■ 外形图及引脚排列




## ■ 极限值（$T_a$=25℃）

$T_{stg}$——贮存温度……-55~175℃

$T_j$——结温…… 175℃

$V_{DSS}$——漏极—源极电压…… 30V

$V_{GS}$——栅极—源极电压…… ±20V

$I_D$——漏极电流（$T_c$=25℃）……100A

$I_{DM}$——漏极电流（脉冲）（注 1）……400A

$P_D$——耗散功率（$T_c$=25℃）……100W

## ■ 电参数（$T_a$=25℃）

| 参数符号 | 符 号 说 明 | 最小值 | 典型值 | 最大值 | 单 位 | 测 试 条 件 |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | 漏—源极击穿电压 | 30 | | | V | $I_D$=250μA ,$V_{GS}$=0V |
| $I_{DSS}$ | 零栅压漏极电流 | | | 1 | μA | $V_{DS}$ =30V，$V_{GS}$=0 |
| $I_{GSS}$ | 栅极泄漏电流 | | | ±100 | nA | $V_{GS}$=±20V ， $V_{DS}$ =0V |
| $V_{GS(th)}$ | 栅—源极开启电压 | 1.0 | | 3.0 | V | $V_{DS}$ = $V_{GS}$ ， $I_D$ =250μA |
| $R_{DS(on)}$ | 漏—源极导通电阻 | | 3.3 | 5.3 | mΩ | $V_{GS}$=10V， $I_D$ =50A |
| $R_{DS(on)}$ | 漏—源极导通电阻 | | 4.8 | 8 | mΩ | $V_{GS}$=4.5V， $I_D$ =40A |
| Ciss | 输入电容 | | 3550 | | pF | $V_{DS}$=25V， $V_{GS}$=0, f=1MHz |
| Coss | 输出电容 | | 1350 | | pF | |
| Crss | 反向传输电容 | | 120 | | pF | |
| $t_{d(on)}$ | 导通延迟时间 | | 11 | | nS | $V_{DS}$ =20V, $V_{GS}$=10V R =0.75Ω $R_G$= 3Ω （注 2） |
| tr | 上升时间 | | 10 | | nS | |
| $t_{d(off)}$ | 断开延迟时间 | | 38 | | nS | |
| $t_f$ | 下降时间 | | 11 | | nS | |
| Qg | 栅极总电荷 | | 48 | | nC | $V_{DS}$ =15V |
| Qgs | 栅极—源极电荷 | | 11 | | nC | $V_{GS}$=10V |
| Qgd | 栅极—漏极电荷 | | 10 | | nC | $I_D$=20A （注 2） |
| $V_{SD}$ | 源极—漏极二极管导通电压 | | | 1.2 | V | $I_S$ =20A ， $V_{GS}$=0 |
| Rth（j-c） | 热阻 | | | 1.5 | ℃/W | 结到外壳 |

*注 1：漏极电流受最大结温限制。

*注 2：脉冲测试，宽度≤300μS,占空比≤2%

## ■ 特性曲线

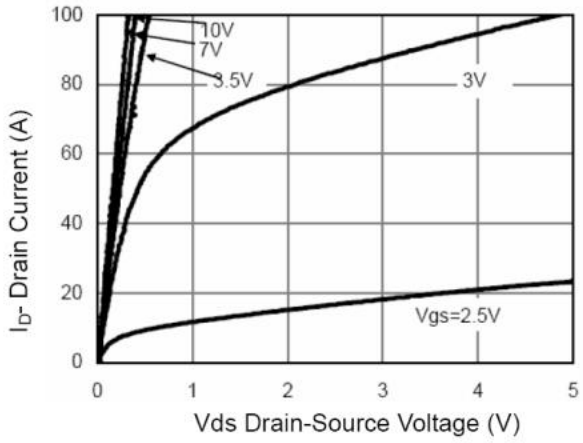



**Figure 1 Output Characteristics**

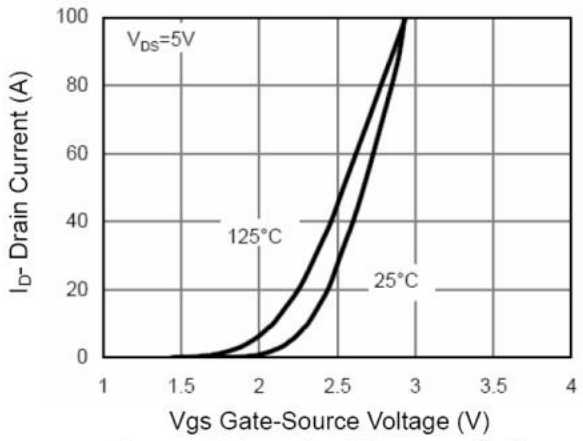



**Figure 2 Transfer Characteristics**

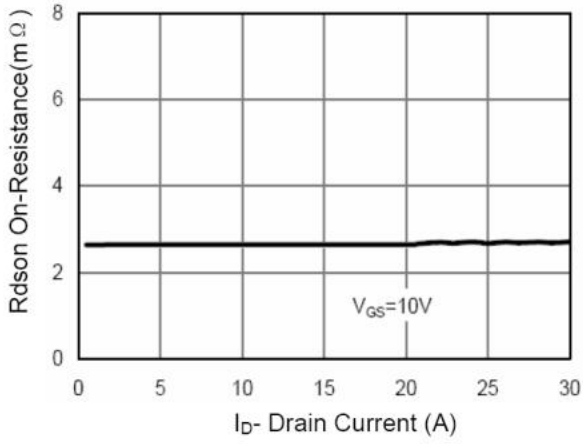



**Figure 3 Rdson- Drain Current**

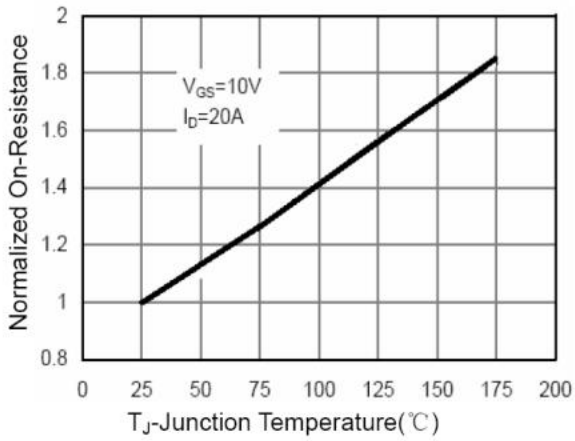



**Figure 4 Rdson-Junction Temperature**

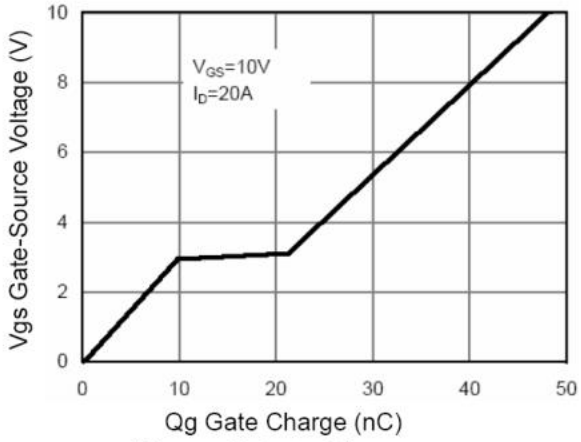



**Figure 5 Gate Charge**

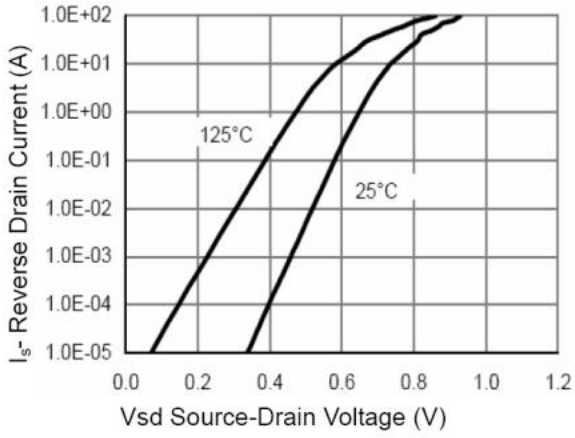



**Figure 6 Source- Drain Diode Forward**

## ■ 特性曲线

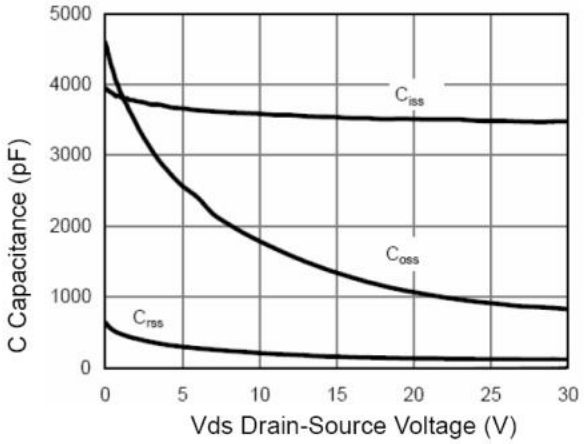



**Figure 7 Capacitance vs Vds**

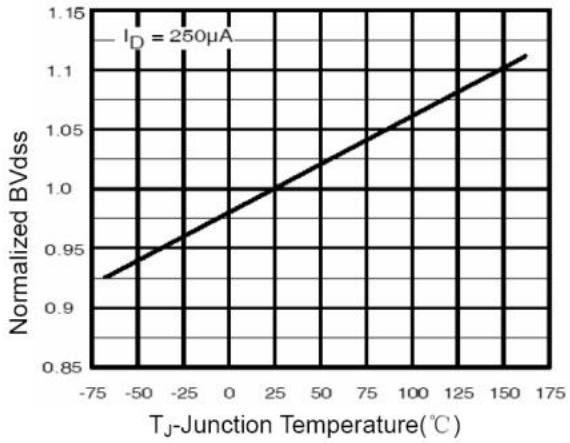



**Figure 9 $BV_{DSS}$ vs Junction Temperature**

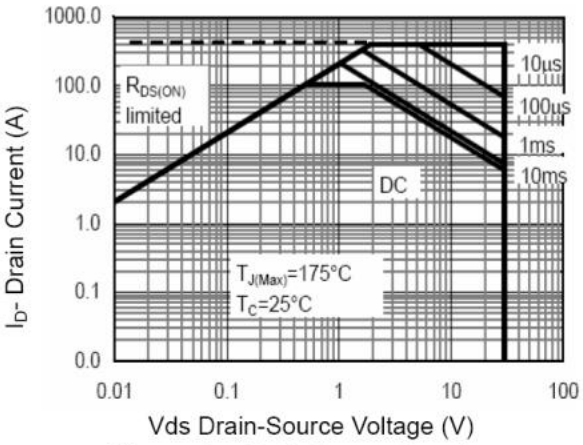



**Figure 8 Safe Operation Area**

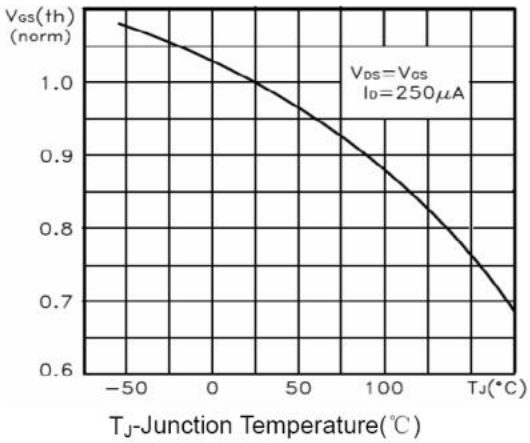



**Figure 10 $V_{GS(th)}$ vs Junction Temperature**

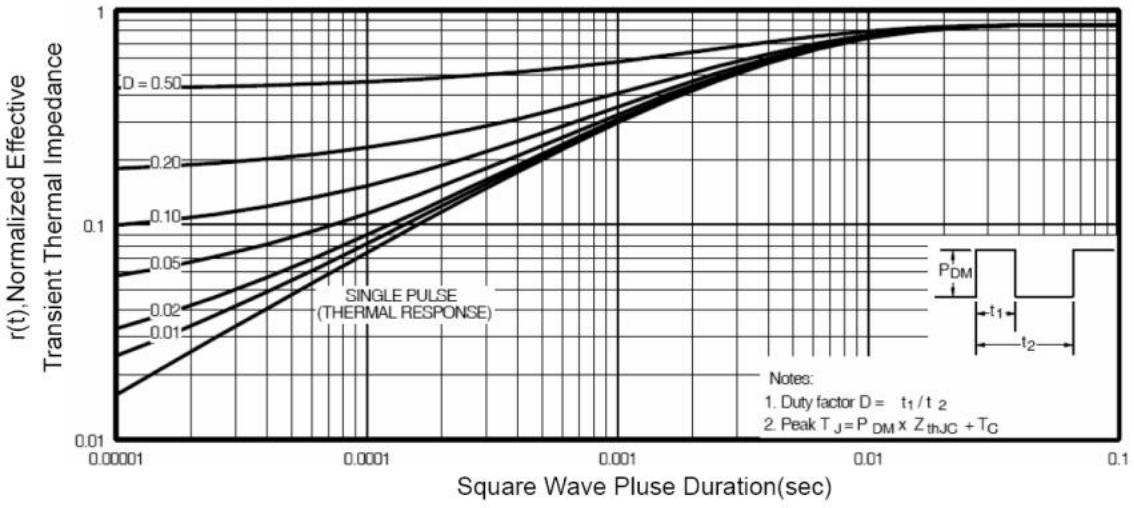
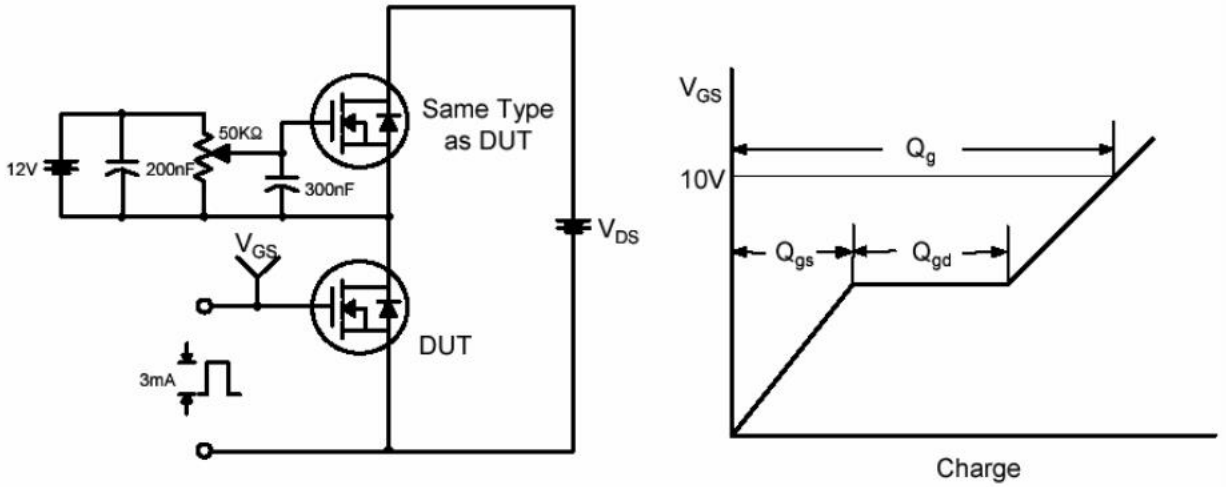


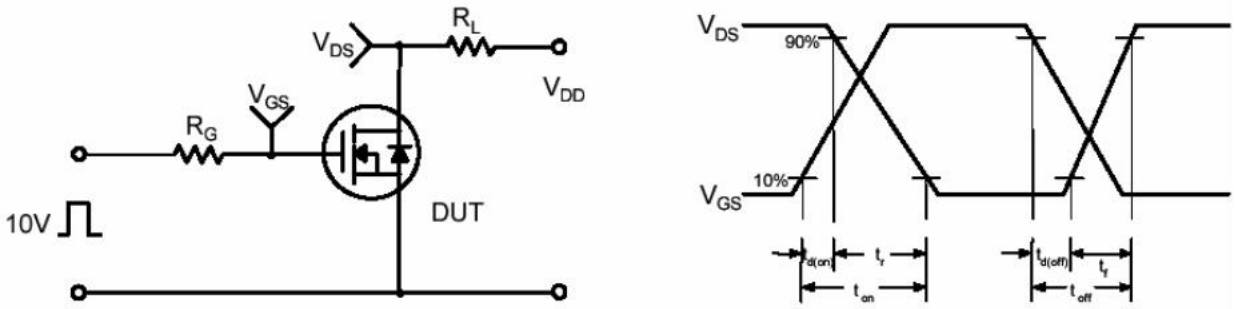

**Figure 11 Normalized Maximum Transient Thermal Impedance**

## ■ 特性曲线

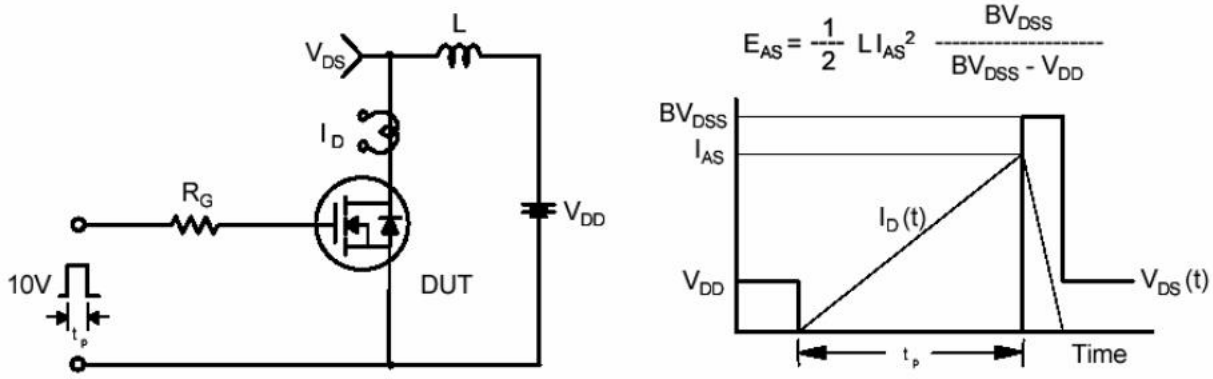
**Gate Charge Test Circuit & Waveform**




**Resistive Switching Test Circuit & Waveforms**




**Unclamped Inductive Switching Test Circuit & Waveforms**



■ 特性曲线

**Peak Diode Recovery dv/dt Test Circuit & Waveforms**